IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S):	Eugene A. Fitzgerald		
SERIAL NO.:	10/022,689	GROUP NO.:	2813
FILING DATE:	December 17, 2001	EXAMINER:	Laura M. Schillinger
TITLE:	CONTROLLING THREADING DISLOCATION DENSITIES IN Ge ON Si USING GRADED GeSi LAYERS AND PLANARIZATION		

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Washington, D.C. 20231-1450

RESPONSE TO OFFICE ACTION

Sir:

This paper is submitted in response to the Office Action mailed on August 9, 2004. In the Office Action, the Examiner requests that we point out where the specification describes "processing the graded region so as to introduce a second [type] of strain."

As noted in the amendment filed on May 13, 2003, which originally introduced this language, support is found at least at page 3, lines 3-6, and page 10, line 17 to page 11, line 3 of the specification. In particular, at page 3, lines 3-6, the application states:

> In another embodiment of the invention there is provided a semiconductor structure comprising a silicon substrate, and a GeSi graded region grown on the silicon substrate, compressive strain being incorporated in the graded region to offset the tensile strain that is incorporated during thermal processing.

And beginning at page 10, line 17, the application states:

> In sample A, the calculated strain due to thermal mismatch when cooling to room temperature is 2.6×10^{-3}, resulting in a high density of surface cracks. When growing sample D, growth modifications specifically designed to alleviate this cracking problem are added. By grading at twice the rate, the total amount of deposited material and the strain energy from the thermal stress accordingly is decreased. More importantly, the fast grading rate at lower temperature and the final Ge concentration jump in sample D, from 92% to 100%, incorporate metastable compressive residual stress into the buffer at the growth temperature. Since the compressive lattice mismatch opposes the tensile thermal mismatch, sample D is left in a nearly stress-free state at room temperature.

Accordingly, in the exemplary discussion, the second type of strain is tensile strain; the processing that causes the tensile strain is thermal processing; and the first type of strain incorporated to offset the second type of strain is compressive strain. Further information concerning the thermal processing leading to tensile strain is found at page 7, lines 2-10. Of course, those of skill in the art would appreciate that tensile strain could just as easily be incorporated to offset process-induced compressive strain. The inventor's contribution lies in solving the problem of process-induced strain by incorporating a different type of strain to counteract it.

In light of the foregoing, we submit that all claims are in condition for allowance. Please charge any fee occasioned by this paper to our Deposit Account No. 20-0531.

Respectfully submitted,

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Reg. No. 33,497

Steven J. Frank
Attorney for Applicant(s)
Testa, Hurwitz, & Thibeault, LLP
High Street Tower
125 High Street
Boston, Massachusetts 02110

Tel. No.: (617) 310-8108
Fax No.: (617) 248-7100